

Rajit Manohar

*Computer Systems Laboratory
School of Electrical and Computer Engineering
Cornell University
Ithaca, NY 14853*

*Office: (607) 255-3553
Fax: (607) 255-9072
<http://vlsi.cornell.edu/~rajit/>
rajit@csl.cornell.edu*

Education:

- Ph.D. 1998 California Institute of Technology
Thesis: **The Impact of Asynchrony on Computer Architecture**
Advisor: *Alain J. Martin*
- M.S. 1995 California Institute of Technology
- B.S. 1994 California Institute of Technology
Advisor: *K. Mani Chandy*

Research Interests:

- Research group: <http://vlsi.cornell.edu/>
- Asynchronous VLSI design and architecture
 - Efficient computation structures
 - Neural information processing

Professional Experience:

- 4/2004 **Associate Professor, ECE** **Cornell University**
Founder, Computer Systems Lab. Affiliations: Computer Science, Electrical and Computer Engineering, Applied Mathematics, Cognitive Studies.
- 8/1998 **Assistant Professor, ECE** **Cornell University**
- 1995–1998 **Research Assistant** **California Institute of Technology**
- 8/2005 **Visiting Scientist** **Massachusetts Institute of Technology**
Microsystems Technology Laboratories
- 10/2004 **Founder and Chief Technology Officer** **Achronix Semiconductor**

Honors, Awards, and Memberships:

- Best paper award at HPEC, 2006
Elected Fellow of the World Technology Network, 2006
Globus Indus Technovators Award, 2006
Invited participant, NAE Frontiers of Engineering Symposium, 2006
Best paper award at ASYNC, 2006
IEEE Fred Ellersick Award for best unclassified paper at MILCOM, 2005
MIT Technology Review's Top 35 Young Innovators under 35 (TR35), 2005
Ruth and Joel Spira Excellence in Teaching Award, 2004–2005
Michael Tien '72 Excellence in Teaching Award, 2003–2004
MIPS paper in Caltech Computer Science 25th Anniversary Selected Bibliography, 2001
Sonny Yau '72 Excellence in Teaching Award, 2000–2001
Cornell University IEEE Teacher of the Year Award, 2000–2001
NSF CAREER award, 2000–2004
Tau Beta Pi and Cornell Society of Engineers Excellence in Teaching Award, 1999–2000
National Semiconductor Corporation Graduate Fellowship, 1996–97
Caltech Merit Award, 1993–94
IIT Academic Award for being ranked 1st in the Institute, 1991 and 1992
Gold Medal, National Standard Examination in Physics (India), 1990

Member: Tau Beta Pi

Member: IEEE Computer Society; Association for Computing Machinery

Professional Activities:

Research:

Associate Editor

IEEE Transactions on VLSI, 2007–

Program Co-Chair

11th International Symposium on Asynchronous Circuits and Systems, March 2005

Program Topic Co-Chair

Conference on Design Automation and Test in Europe, March 2003

Program Committees

International Conference on Computer Design, October 2006

International Conference on Computer Aided Design, November 2005

Conference on Design Automation and Test in Europe, March 2005

2nd IEEE Upstate NY Workshop on Sensor Networks, October 2003

16th International Conference on Supercomputing, June 2002

7th–13th International Symposium on Asynchronous Circuits and Systems, 2001–2007

Co-Organizer

Workgroup on Address-Event Representation, NSF Workshop on Neuromorphic Engineering

Telluride, CO, July 2000

Proposal/Panel/Program Reviewer

National Science Foundation; Army Research Office; US-Israel Binational Science Foundation; IWT

Brussels, Belgium; Singapore National Research Foundation

Conference/Workshop Reviewer

Conference on Advanced Research in VLSI; Design Automation Conference; EuroPar; International

Conference on Parallel Architectures and Compilation Techniques; International Parallel Process-

ing Symposium; International Parallel and Distributed Processing Symposium; International Sym-

posium on Asynchronous Circuits and Systems; International Symposium on High Performance

Computer Architecture; International Symposium on Operating System Principles; Workshop on

Asynchronous Design Methodologies; Workshop on System Area Networks

Journal Reviewer

ACM Transactions on Programming Languages and Systems; Formal Aspects of Computing; IEEE

Computer; IEEE Transactions on Circuits and Systems; IEEE Transactions on Computer Aided

Design; IEEE Transactions on Computers; IEEE Transactions on VLSI; Information Processing

Letters; INTEGRATION: The VLSI Journal; Proceedings of the IEEE

Industry:

Founder and Chief Technology Officer, Achronix Semiconductor

Startup company commercializing asynchronous FPGAs. 10/2004–

Consulting

ATC-NY. Asynchronous logic synthesis (DARPA/SBIR). 1/2003–9/2003

URU Technologies. Low power embedded systems. 12/2004, 9/2005

Talks:

Invited talks:

“Microprocessor Forum.” Invited panelist, Gilder-Forbes Telecom Conference, Lake George, NY,

May 2008.

“The Critical Path of Fiberspeed Connectivity: Flexible vs. Fixed Silicon Solutions.” Invited panelist, Gilder-Forbes Telecosm Conference, Lake George, NY, October 2007.

“The Implications of Fast Asynchronous Reconfigurable Logic.” Workshop on Terascale Integration, Defence Science Research Council, Washington, DC, October 2007.

“3D Integrated Circuits: A Designer’s Perspective.” Keynote panelist, 24th VLSI Multilevel Interconnection Conference. Fremont, CA, September 2007.

“Fast Reconfigurable Logic.” Invited seminar, Yale University, September 2007.

“Asynchronous FPGAs.” Keynote, Workshop on Unique Chips and Systems, San Jose, CA, April 2007.

“Reconfigurable Asynchronous Logic.” University of Texas at Austin, Austin, TX, March 2007.

“Asynchronous Embedded Systems.” Welch-Allyn, Skeneateles, NY, March 2007.

“Asynchronous Circuits and Systems.” Pomona College, CA, November 2006.

“Reconfigurable Asynchronous Logic.” Custom Integrated Circuits Conference, San Jose, CA, September 2006.

“Self-timed Systems.” Microsystems Technology Labs, MIT, Boston, MA, December 2005.

“Reconfigurable Asynchronous Logic.” Columbia University, New York, NY, December 2005.

“Asynchronous FPGAs.” Air Force Rome Labs, Rome, NY, October 2005.

“Reconfigurable Asynchronous Logic.” Olin College, MA, October 2005.

“Architectures for Cognitive Systems.” Workshop on Cognitive Architectures and Systems, Ithaca, NY, July 2005.

“Hardware/software co-design for Sensor Networks.” Second International Workshop on Networked Sensing Systems, San Diego, CA, June 2005.

“Asynchronous Logic for Extreme Environments.” University of Central Florida, Orlando, FL, May 2005.

“Asynchronous FPGAs.” Xilinx Research Labs, San Jose, CA, April 2005.

“Activity-Driven Asynchronous Circuits and Systems.” IGERT Seminar on Machines and Organisms, Ithaca, NY, February 2005.

“Issues in the Design of Sensor Network Processors.” NSF Meeting on Networks of Sensor Systems, October 2004.

“Sensor Networks and Asynchronous VLSI.” IEEE Computer Society Symposium on VLSI, February 2004.

“How Asynchronous should we be?” Invited panelist, IEEE Computer Society Symposium on VLSI, February 2004.

“Ultra Low Power Asynchronous VLSI.” DARPA Workshop on Ultra Low Power Technologies, MIT, January 2004.

“Asynchronous Event-Processing.” Analog and Biological VLSI Systems Seminar, MIT, November 2003.

“SNAP: A Sensor Network Asynchronous Processor.” Electrical and Systems Engineering Colloquium, University of Pennsylvania, October 2003.

“Designing an Efficient Sensor Network Processor.” VLSI seminar series, School of Electrical and Computer Engineering, Cornell University, September 2003.

“Modeling Wireless Networks with Asynchronous VLSI.” Information Sciences Seminar, California Institute of Technology, Pasadena, CA, June 2002.

“Why we should design asynchronous circuits.” Intel Microprocessor Research Labs, Hillsboro, OR, April 2002.

“Network Simulation with Asynchronous VLSI.” Portland State University, Portland, OR, April 2002.

“Network Simulation with Asynchronous VLSI.” AT&T Research Labs, Menlo Park, CA, January 2002.

“Scalable Formal Design Methods for Asynchronous VLSI.” Keynote talk, 29th Annual ACM SIGPLAN/SIGACT Symposium on Principles of Programming Languages, Portland, OR, January 2002.

“Asynchronous VLSI for Wireless Communication Systems.” Plenary talk, IEEE Circuits and Systems Workshop on Wireless Communications and Networking, Notre Dame, IN, August 2001.

“Low Energy Adaptive Processors.” Cornell Computer Science Distinguished Lecture Series, Ithaca, NY, September 2000.

“Asynchronous VLSI Design.” NSF Workshop on Neuromorphic Engineering, Telluride, CO, July 2000.

“A Methodology for Designing Asynchronous Circuits.” PRL Seminar, CS, Cornell, January 1999.

“Slack Elasticity in Asynchronous Systems.” Compaq’s Systems Research Center, Palo Alto, CA, April 1998.

“High-performance asynchronous microprocessors.” Cornell University (and others), March 1998.

“The design of asynchronous adders.” Seminar, ECE Department, Johns Hopkins University, June 1997.

“Quasi-Delay-Insensitive Circuits are Turing-Complete.” International Symposium on Advanced Research in Asynchronous Circuits and Systems, Aizu-Wakamatsu, Japan, March 1996.

“Asynchronous Circuit Design.” Digital’s Systems Research Center, Palo Alto, CA, September 1995.

Conference presentations:

“Application of Low Power, High Density, Gigahertz Speed Commercial FPGA Technology to High Radiation Applications using RADHARD-by-Process Techniques.” *9th Military and Aerospace Programmable Logic Devices International Conference*, Washington, DC, September 2006.

“A High-Performance Asynchronous FPGA: Test Results.” IEEE Symposium on Field-Programmable Custom Computing Machines, Napa, CA, April 2005.

“Asynchronous Logic for Cryogenic Applications.” IMAPS Advanced Technology Workshop on Reliability of Advanced Electronic Packages and Devices in Extreme Cold Environments, Pasadena, CA, February 2005.

“Delta Dataflow Networks for Event Stream Processing.” Proceedings of the 16th IASTED International Conference on Parallel and Distributed Computing and Systems, November 2004.

“Width-Adaptive Data Word Architectures.” 19th Conference on Advanced Research in VLSI, March 2001.

“An Analysis of Reshuffled Handshaking Expansions.” Seventh International Symposium on Asynchronous Circuits and Systems, March 2001.

“A Case for Asynchronous Computer Architecture.” ISCA Workshop on Complexity-Effective Design, Vancouver, BC, June 2000

“Slack Elasticity in Concurrent Computing.” Fourth International Conference on the Mathematics of Program Construction, Maarstrand, Sweden, June 1998

University Activities:

Member, Technology Transfer Advisory Committee, Cornell, 2008–

Member, Operations Oversight Subcommittee for technology transfer office, 2008–

Member, Mediation Subcommittee for grievances, 2008–
 Member, Review committee for graduate admissions requirements, Cornell, 2008–
 Director of Graduate Studies, ECE, Cornell, 2007–
 Search Committee for ECE Director, Cornell, 2007–2008
 Graduate Admissions Advisory Board, Cornell, 2005
 College of Engineering Teaching Awards Committee, Cornell, 2003
 ECE Graduate Committee, Cornell, 1999–2001, 2003–2004
 ECE Targeted Faculty Recruiting Committees, Cornell, 1998–2001, 2003–2006
 ECE General Faculty Recruiting Committee, Cornell, 2001–2003
 ECE Policy Committee, Cornell, 2001–2003, 2003–2004, vice chair 2004–2005
 CAM Computer Committee, Cornell, Chair 2001–2004
 CIT Packet Shaping Advisory Committee, Cornell, 2002
 ECE Computing Committee, Cornell, 1999–2001

Teaching Experience:

2004–	Associate Professor	Cornell University
	<i>Instructor:</i> ECE 574: Advanced Digital VLSI Design (12 in S04; 8 in F04; 19 in F07) ECE 571: Arithmetic Circuits ECE 320: Systems and Networks (116 in S05)	
1998–2004	Assistant Professor	Cornell University
	<i>Instructor:</i> ECE 574/6: Advanced Digital VLSI Design (29 in S02; 15 in S03; 20 in F07) EE 571: Asynchronous VLSI Design (15 in F98; 25 in F99; 24 in F00) ECE 474: Digital VLSI Design (66 in F01/S02; 66 in F02/S03; 95 in F03/S04) EE/CS 314: Computer Organization (205 in S00; 305 in S01) <i>Assisted:</i> EE 439: Digital VLSI System Design (~30 in F98) EE 308: Fund. of Comp. Engr. (~80 in S99) EE 475: Computer Architecture (104 in F99)	
1996–97	Instructor	California Institute of Technology
	Taught a three-term graduate-level course: Concurrency in Computation (CS139abc).	
1993–98	Teaching Assistant	California Institute of Technology
	Computers, Computation, and Programs (CS20); Design and Implementation of Programming Languages (CS237); Asynchronous VLSI Design Laboratory (CS185); Digital VLSI Design Laboratory (CS/EE181).	
2002–2005	Explorations in Engineering	Cornell University
	Faculty participant in Cornell's summer program for high school juniors/seniors.	
2000–2001	CURIE Academy	Cornell University
	Faculty participant in Cornell's summer program for high school women that excel in math and science.	
1996–98	Mentor Scientist	Caltech Pre-College Science Initiative
	Student volunteer for Caltech's high school teacher training program.	

1994–95 **CRPC Summer Intern Advisor** **California Institute of Technology**
 Suggested projects and helped supervise summer interns in the Center for Research
 on Parallel Computation summer internship program for women and minorities.

Advising:

Graduate Field Memberships:

Electrical and Computer Engineering; Computer Science; Applied Mathematics

Ph.D. theses supervised:

David Fang (Ph.D., May 2008). *A Profiling Infrastructure for Performance Evaluation of Asynchronous Systems*. First employment: Achronix Semiconductor Corp

David Biermann (Ph.D., September 2006). *A Workload Adaptive Voltage Scaling Multiple Clock Domain Architecture*. First employment: Intel, Portland, OR

Song Peng (Ph.D., August 2006). *Implementing Self-Healing Behavior in Quasi Delay-Insensitive Circuits*. First employment: Cadence

Virantha Ekanayake (Ph.D., May 2005). *Dynamic Significance Compression in a Sensor Network Asynchronous Processor*. First employment: Assistant Professor, Johns Hopkins University

Clinton Kelly, IV (Ph.D., May 2005). *The Design and Implementation of an Asynchronous Network on a Chip*. First employment: Co-founder, Achronix Semiconductor Corporation

John Teifel (Ph.D., May 2004). *Fast Prototyping of Asynchronous Logic*. First employment: Senior Member of the Technical Staff, Sandia National Labs

M.S. theses supervised:

Chris LaFrieda (M.S., August 2005). *Custom Quality Leaf Cell Routing Using Modern Design Rules*.

Filipp Akopyan (M.S., August 2005). *Asynchronous Analog-to-Digital Conversion*.

David Fang (M.S., October 2003). *Designing Asynchronous Register Files*.

David Biermann (M.S., December 2002). *Multiprocessor-Enabled Asynchronous Cache Controller*.

Clinton Kelly IV (M.S., November 2002). *Wireless Network Simulation Done Faster than Real Time*.

Virantha Ekanayake (M.S., November 2002). *Asynchronous DRAM Design and Implementation*.

John Teifel (M.S., May 2002). *Interchip Communication in Asynchronous VLSI Systems*.

Current graduate student advisees:

Christopher LaFrieda (Ph.D., ECE). *September 2002–August 2008*. Topic: Fault-Tolerant Asynchronous Circuits

Filipp Akopyan (Ph.D., ECE). *August 2004–May 2008*. Topic: Asynchronous Signal Processing

Sandra Jackson (Ph.D., ECE). *January 2006–*. Topic: Interfaces Between Asynchronous and Synchronous Circuits

Carlos Tadeo Ortega Otero (Ph.D., ECE). *August 2006–*. Topic: Secure Systems

Basit Sheikh (Ph.D., ECE). *August 2005–*. Topic: Asynchronous Floating-Point Arithmetic

Benjamin Hill (Ph.D., ECE). *September 2007–*. Topic: TBD

Rob Karmazin (Ph.D., ECE). *September 2007–*. Topic: TBD

PUBLICATIONS

(*underlined names are my students*)

Journal Articles:

John Teifel and Rajit Manohar. An Asynchronous Dataflow FPGA Architecture. *IEEE Transactions on Computers*, special issue on Field-Programmable Logic, November 2004.

- Rajit Manohar and Clinton Kelly, IV. Network on a Chip: Modeling Wireless Networks with Asynchronous VLSI. *IEEE Communications Magazine*, Vol. 39, No. 11, pp. 149–155, November 2001.
- Rajit Manohar. The Entropy of Traces in Parallel Computation. *IEEE Transactions on Information Theory*, **45**(5):1606–1608, July 1999.
- K. Rustan M. Leino and Rajit Manohar. Joining Specification Statements. *Theoretical Computer Science*, **216**:375–394, March 1999.
- Rajit Manohar and José A. Tierno. Asynchronous Parallel Prefix Computation. *IEEE Transactions on Computers*, **47**(11):1244–1252, November 1998.
- Donald Dabdub and Rajit Manohar. Performance and Portability of an Air Quality Model. *Parallel Computing*, Special Issue on Regional Weather Models, **23**(14):2187–2200, 1997.
- Rajit Manohar and K. Rustan M. Leino. Conditional Composition. *Formal Aspects of Computing*, **7**(6):683–703, 1995.

Articles in Major Conferences:

- Christopher LaFrieda, Engin Ipek, Jose Martinez, and Rajit Manohar. Utilizing dynamically coupled cores to form a resilient chip multiprocessor. *Proceedings of the International Conference on Dependable Systems and Networks*, June 2007.
- Rajit Manohar. Reconfigurable Asynchronous Logic. *Proceedings of the IEEE Custom Integrated Circuits Conference*, September 2006.
- Song Peng and Rajit Manohar. Yield enhancement of asynchronous logic circuits through 3-dimensional integration technology. *Proceedings of the ACM Great Lakes Symposium on VLSI*, April 2006.
- Song Peng and Rajit Manohar. Self-healing Asynchronous Arrays. *Proceedings of the 12th IEEE International Symposium on Asynchronous Circuits and Systems*, March 2006.
- Filipp Akopyan, Rajit Manohar, and Alyssa Apsel. A level-crossing Flash Asynchronous Analog-to-Digital Converter. *Proceedings of the 12th IEEE International Symposium on Asynchronous Circuits and Systems*, March 2006.
- David Fang, Filipp Akopyan, and Rajit Manohar. Self-Timed Thermally Aware Circuits. *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, Karlsruhe, March 2006.
- Yao-Win Hong, Anna Scaglione, Rajit Manohar, and Birsen Sirkeci-Mergen. Dense Sensor Networks are also Energy-efficient: when ‘more’ is ‘less’. *Proceedings of MILCOM 2005*, October 2005.
- Song Peng and Rajit Manohar. Efficient Failure Detection in Pipelined Asynchronous Circuits. *Proceedings of the IEEE Symposium on Defect and Fault Tolerance in VLSI Systems*, October 2005.
- Song Peng and Rajit Manohar. Fault Tolerant Asynchronous Adders through Dynamic Self-reconfiguration. *Proceedings of the IEEE International Conference on Computer Design*, October 2005.
- Christianto C. Liu, Jeng-Huei Chen, Rajit Manohar, and Sandip Tiwari. Mapping Multimedia Applications to 3-D System-on-Chip. *Proceedings of the 2005 IEEE International Symposium on Circuits and Systems*, May 2005.
- David Fang, John Teifel, and Rajit Manohar. A High-Performance Asynchronous FPGA: Test Results. *2005 IEEE Symposium on Field-Programmable Custom Computing Machines*, April 2005.
- Song Peng, David Fang, John Teifel, and Rajit Manohar. Automated Synthesis for Asynchronous FPGAs. *13th ACM International Symposium on Field-Programmable Gate Arrays*, March 2005.

- Virantha Ekanayake, Clinton Kelly, IV, and Rajit Manohar. BitSNAP: Dynamic Significance Compression for a Low-Energy Sensor Network Asynchronous Processor. *Proceedings of the 11th IEEE International Symposium on Asynchronous Circuits and Systems*, March 2005.
- Virantha Ekanayake, Clinton Kelly, IV, and Rajit Manohar. An Ultra Low Power Processor for Sensor Networks. *Proceedings of the Eleventh International Symposium on Architectural Support for Programming Languages and Operating Systems*, October 2004.
- Christopher LaFrieda and Rajit Manohar. Fault Detection and Isolation Techniques for Quasi Delay-Insensitive Circuits. *Proceedings of the International Conference on Dependable Systems and Networks*, June 2004.
- John Teifel and Rajit Manohar. Static Tokens: Using Dataflow to Automate Concurrent Pipeline Synthesis. *Proceedings of the 10th International Symposium on Asynchronous Circuits and Systems*, April 2004.
- David Fang and Rajit Manohar. Non-Uniform Access Asynchronous Register Files. *Proceedings of the 10th International Symposium on Asynchronous Circuits and Systems*, April 2004.
- John Teifel and Rajit Manohar. Highly Pipelined Asynchronous FPGAs. *12th ACM International Symposium on Field-Programmable Gate Arrays*, February 2004.
- Clinton Kelly IV and Rajit Manohar. An Event-Synchronization Protocol for Parallel Simulation of Large-Scale Wireless Networks. *IEEE Symposium on Real Time and Distributed Simulation*, October 2003.
- John Teifel and Rajit Manohar. Programmable Asynchronous Pipeline Arrays. *Proceedings of the 13th International Conference on Field Programmable Logic and Applications*, September 2003.
- Rajit Manohar and Anna Scaglione. Power Optimal Routing in Wireless Networks. *IEEE International Conference on Communications*, pp. 2979–2984, May 2003.
- Virantha Ekanayake and Rajit Manohar. Asynchronous DRAM Design and Synthesis. *Proceedings of the Ninth International Symposium on Asynchronous Circuits and Systems*, pp. 174–183, May 2003.
- John Teifel and Rajit Manohar. A High Speed Clockless Serial Link Transceiver. *Proceedings of the Ninth International Symposium on Asynchronous Circuits and Systems*, pp. 151–161, May 2003.
- Clinton Kelly, IV, Virantha Ekanayake, and Rajit Manohar. SNAP: A Sensor Network Asynchronous Processor. *Proceedings of the Ninth International Symposium on Asynchronous Circuits and Systems*, pp. 24–33, May 2003.
- John Teifel, David Fang, David Biermann, Clinton Kelly, IV, and Rajit Manohar. Energy-Efficient Pipelines. *Proceedings of the Eighth International Symposium on Asynchronous Circuits and Systems*, pp. 21–31, March 2002.
- Rajit Manohar. Scalable Formal Design Methods for Asynchronous VLSI. Invited article, *Proceedings of the 29th Annual ACM SIGPLAN/SIGACT Symposium on Principles of Programming Languages*, January 2002.
- Rajit Manohar. Width-Adaptive Data Word Architectures. *Proceedings of the 2001 Conference on Advanced Research in VLSI*, pp. 112–129, March 2001.
- Rajit Manohar, Mika Nyström, and Alain J. Martin. Precise Exceptions in Asynchronous Processors. *Proceedings of the 2001 Conference on Advanced Research in VLSI*, pp. 16–28, March 2001.
- Rajit Manohar. An Analysis of Reshuffled Handshaking Expansions. *Proceedings of the Seventh International Symposium on Asynchronous Circuits and Systems*, pp. 96–105, March 2001.

Rajit Manohar, Tak-Kwan Lee, and Alain J. Martin. Projection: A Synthesis Technique for Concurrent Systems. *Proceedings of the Fifth International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pp. 125–134, April 1999.

Rajit Manohar and Alain J. Martin. Slack Elasticity in Concurrent Computing. *Proceedings of the Fourth International Conference on the Mathematics of Program Construction*, Lecture Notes in Computer Science 1422, pp. 272–285, Springer-Verlag, June 1998.

Alain J. Martin, Andrew Lines, Rajit Manohar, Mika Nyström, Paul Penzes, Robert Southworth, Uri V. Cummings, and Tak-Kwan Lee. The Design of an Asynchronous MIPS R3000 microprocessor. *Proceedings of the 17th Conference on Advanced Research in VLSI*, pp. 164–181, September 1997.

José A. Tierno, Rajit Manohar, and Alain J. Martin. The Energy and Entropy of VLSI Computations. *Proceedings of the Second International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pp. 188–196, March 1996.

Rajit Manohar and Alain J. Martin. Quasi-delay-insensitive circuits are Turing-complete. Invited article, *Second International Symposium on Advanced Research in Asynchronous Circuits and Systems*, March 1996. Available as Caltech technical report CS-TR-95-11, November 1995.

K. Mani Chandy, Rajit Manohar, Berna L. Massingill, and Daniel I. Meiron. Integrating Task and Data Parallelism using the Group Communication Archetype. *Proceedings of the Ninth International Parallel Processing Symposium*, pp. 724–733, 1995.

Articles in Other Conferences and Workshops:

Rajit Manohar, Clinton W. Kelly, IV, John Lofton Holt, Chris Liu, Leonard Rockett, Dinu Patel, Steven Danziger, S. Ramaswamy, Ken LaBel. Reconfigurable, High Density Gigahertz Speed Low Power Radiation Hardened FPGA Technology. *Military and Aerospace FPGA and Applications Meeting*, November 2007.

Rajit Manohar, Clinton W. Kelly, IV, John Lofton Holt, Chris Liu, Leonard Rockett, Dinu Patel, Steven Danziger. Development of Reprogrammable, Low Power, High Density, High Speed RADHARD FPGAs using Proven Commercial Technology and RADHARD-by-Process Techniques. *Government Microcircuit Applications and Critical Technology Conference*, Lake Buena Vista, FL, March 2007.

David Fang, Christopher LaFrieda, Song Peng, and Rajit Manohar. A 3-Tier Asynchronous FPGA. *Proc. 23rd International VLSI/ULSI Multilevel Interconnection Conference*, September 2006.

Jon Russo, Mohammed Amduka, Keith Pendersen, Richard Lethin, Jonathan Springer, Rajit Manohar, Rami Melhem. Enabling Cognitive Architectures for UAV Mission Planning. *Proceedings of the High Performance Embedded Computing Workshop*, September 2006.

Rajit Manohar, Clinton W. Kelly, IV, John Lofton Holt, Chris Liu, Leonard Rockett, Dinu Patel, Steven Danziger. Application of Low Power, High Density, Gigahertz Speed Commercial FPGA Technology to High Radiation Applications using RADHARD-by-Process Techniques. *9th Military and Aerospace Programmable Logic Devices International Conference*, Washington, DC, September 2006.

Rajit Manohar. Asynchronous Logic for Cryogenic Applications. *IMAPS Advanced Technology Workshop on Reliability of Advanced Electronic Packages and Devices in Extreme Cold Environments*, Pasadena, CA, February 2005.

Rajit Manohar and K. Mani Chandy. Δ -dataflow Networks for Event Stream Processing. *Proc. IASTED International Conference on Parallel and Distributed Computing and Systems*, November 2004.

David Biermann, Emin Gün Sirer, and Rajit Manohar. A Rate Matching-based Approach to Dynamic Voltage Scaling. *Proc. First Watson Conference on the Interaction between Architecture, Circuits, and Compilers*, October 2004.

Rajit Manohar. A Case for Asynchronous Computer Architecture. *Proceedings of the ISCA Workshop on Complexity-Effective Design*, June 2000.

Rajit Manohar and Mark Heinrich. A Case for Asynchronous Active Memories. *Proceedings of the ISCA Workshop on Solving the Memory Wall*, June 2000.

Patents:

Caltech

Rajit Manohar and Alain J. Martin. *Parallel prefix operations in asynchronous processors*. US Patent 5,999,961, December 1999.

Rajit Manohar, Mika Nyström, and Alain J. Martin. *Exception Processing in Asynchronous Processors*. US Patent 6,301,655, October 2001.

Alain J. Martin, Andrew Lines, Rajit Manohar, Mika Nyström, Uri Cummings. *Pipelined Asynchronous Processing*. US Patent 6,381,692, April 2002.

Alain J. Martin, Andrew Lines, Rajit Manohar, Mika Nyström, Uri Cummings. *Pipelined Asynchronous Processing*. US Patent 6,658,550, December 2003.

Mika Nyström, Rajit Manohar, and Alain J. Martin. *Method and Apparatus for a Failure-free Synchronizer*. US Patent 6,690,203, February 2004.

Rajit Manohar and Alain J. Martin. *The Branch Processor Architecture*. Patent pending.

Cornell

Rajit Manohar and John Teifel. *Programmable Asynchronous Pipeline Arrays*. US Patent 7,157,934, January 2007.

David Fang, Filipp Akopyan, Rajit Manohar. *Self-Timed Thermally Aware Circuits and Methods of Use Thereof*. US Patent, April 2008.

Rajit Manohar and Clinton Kelly, IV. *Event Synchronization Protocol for Scalable Simulation of Large-Scale Wireless Networks*. CRF #D-3312, #D-3310 Patent pending.

Rajit Manohar and Clinton Kelly, IV. *Sensor-Network Processor Using Event-Driven Architecture*. CRF #D-3309, #D-3310. Patent pending.

Filipp Akopyan, Rajit Manohar, Alyssa B. Apsel. *Architecture for an Asynchronous Analog-to-Digital Converter*. CRF #D-3734. Patent pending.

Other

Rajit Manohar. *Systems and Methods for Performing Automated Conversion of Representations of Synchronous Circuit Designs to and from Representations of Asynchronous Circuit Designs*. Patent pending.

Rajit Manohar and Clinton Kelly, IV. *Fault Tolerant Asynchronous Circuits*. Patent pending.

Rajit Manohar and Clinton Kelly, IV. *Asynchronous Field Programmable Fabric Architecture*. Patent pending.

Rajit Manohar and Clinton Kelly, IV. *Multipath Fault Tolerant Asynchronous Circuits*. Patent pending.

Many others pending.