

ASYNC 2005 Call for Papers

March 14-16, 2005 — New York City, NY, USA

Venue: *Columbia University*

11th IEEE International Symposium on Asynchronous Circuits and Systems

The International Symposium on Asynchronous Circuits and Systems provides a high quality forum for scientists and engineers to present their latest research findings. Authors are invited to submit full papers on all aspects of asynchronous design. Topics of interest include, but are not limited to:

- **Mixed synchronous/asynchronous architectures, interfaces, and circuits**
- **High-speed/low-power asynchronous logic, memories, and interconnects**
- **High-level design and synthesis of self-timed circuits**
- **Physical design of unlocked logic and pipelines**
- **Formal methods for correctness and performance analysis of asynchronous designs**
- **Test, reliability, security, and radiation tolerance**
- **CAD for asynchronous design and validation**
- **Asynchronous System-on-a-chip (SoC)**
- **Novel asynchronous architectures**
- **Asynchrony and latency tolerance in system-level design**

Papers should be submitted via the conference web site. The submission should not exceed ten pages in IEEE double column format. Papers that exceed the length limit may not be reviewed. Papers will be evaluated by the program committee and reviews will be based on scientific merit, innovation, relevance, and presentation. “New-idea” papers are encouraged, and the program committee recognizes that such papers may contain less evaluation than papers in established areas. Accepted papers will be published in a proceedings that will be distributed at the conference. Please check the conference web site for up-to-date information:

<http://vlsi.cornell.edu/async2005/>

Important dates

- Paper submission deadline: **September 27, 2004**
- Author notification: **November 29, 2004**
- Final paper submission: **January 3, 2005**

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