Carlos Tadeo **Ortega Otero**

Sr. Research and Development Engineer

contact

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interests

♥ VLSI, digital circuits, ubiquitous computing, automation, cyber-physical systems, low-energy, & CAD tools

education

2006–2014 **Doctor** of Philosophy — Cornell University, Ithaca, NY

Thesis: Asynchronous Design for Ubiquitous Computing
Advisor: Rajit Manohar
Electrical and Computer Engineering

2006–2012 **Master** of Science — Cornell University, Ithaca, NY

Thesis: Static Power Reduction Techniques for Asynchronous Circuits
Advisor: Rajit Manohar
Electrical and Computer Engineering

2001–2006 **Bachelor** of Science — ITESM-CEM. Mexico, Mexico

Specialization in Computer Engineering
Advisor: Marcos De Alba Rosano

experience

2015–Now **St. Jude Medical, Cardiovascular division** — Atlanta, GA

Sr. Research and Development Engineer

- **Deep implantable electronic sensors**. Designed miniaturized deep-implantable electronic systems to sense biological signals
- **RF power harvesting and power transmission**. Designed efficient near-field RF power transmission and power harvesting circuits and protocols
- **Interrogator design**. Design and implement application-specific RF digital communication circuits, protocols, and interrogators

2014–2015 **Cornell University** — Ithaca, NY

VLSI innovator and Postdoctoral Research Associate

- **On-chip security**. Energy efficient crypto coprocessors for low-energy chips
- **Layout for 28nm and beyond**. Fully automated timing-driven layout for asynchronous circuits in 28nm, 22nm, 16nm, and beyond

2006-2014 **Cornell University** — Ithaca, NY

Graduate Research Assistant

- **Low energy**. Designed and implemented an ultra-low energy microcontroller that uses only 27pJ at 50Mhz or 47pJ at 93Mhz.
- **Zero Static Power consumption**. Designed methodologies to use power-gating techniques in the context of pipelined asynchronous circuits with instantaneous wake-up. 80% idle power reduction
- **Trusted layout**. Developed techniques and automated tools to protect Intellectual Property using obfuscated layout and split-foundry manufacturing
- **Automatic layout**. Designed and implemented a flow to create full-custom quality automated layout for asynchronous circuits

- **3D Integration**. Analyzed challenges and proposed solutions for the next generation of 3-D integrated circuits
- **Test chips**. Designed, fabricated and tested Integrated circuits:
  1. 65nm Split-Foundry FPGA (2014). Fully functional
  2. 130nm Split-Foundry FPGA (2013). Fully functional
  3. 90nm Low power baseband GPS (2012). Partially functional
  4. 90nm Ultra-low Energy Processor (2011). Fully functional
  5. 45nm SOI Cornell-IBM SyNAPSE (2010). Fully functional
  6. 65nm Hybrid processor-FPGA (2010). Fully functional
  7. 0.5um Si-Ge extreme conditions pipeline (2008). Fully functional
  8. 180nm-SOI 3-D Through-Silicon-Via testchip(2008). Fully functional

2012 **International Business Machines (IBM)** Yorktown Heights, NY

Layout automation consultant, asynchronous circuit consultant
As part of the Cognitive Computing Group at IBM, I contributed to the SyNAPSE project.

- Aid on the integration of SyNAPSE– the largest chip ever built by IBM
- Verification and integration of asynchronous cycle-accurate simulators

2006 **Softtek** Mexico City, Mexico

Junior Programmer, Object Oriented Designer

- Assigned as an external consultant to Banamex
- Responsible for building controllers for printers and Pin Pads
- Built the infrastructure for Corresponsales Banamex

publications g+

h-index:6 i10-index:4

1. Automated Obfuscated Layout for Trusted Split-Foundry Design

Ortega, C. J. Tse, R. Karmazin, B. Hill, Manohar R.

Symposium on Hardware Oriented Security and Trust (HOST) (2015). 2015

2. ULSNAP: An Ultra-Low Power Event-Driven Microcontroller for Sensor Network Nodes

Ortega, C. J. Tse, R. Karmazin, B. Hill, Manohar R.

International Symposium on Quality Electronic Design (ISQED) (2014). 2014

3. A Split-Foundry Asynchronous FPGA

B. Hill, R. Karmazin, **Ortega, C.** J. Tse, Manohar R.

International Symposium on Quality Electronic Design (2014). 2014

4. cellTK: Automated Layout for Asynchronous Circuits with Nonstandard Cells

R. Karmazin, **Ortega, C.** Manohar R.

International Symposium on Asynchronous Circuits and Systems (ASYNC) (2013). 2013

5. Dynamic electrothermal simulation of three dimensional Integrated Circuits using Standard Cell Macromodels

S. Priyadarshi, R. Harris, S. Melamed, **Ortega, C.** N Kriplani, C N. Christoffersen, R Manohar, S. Dooley, W Davis, P Franzon, M Steer

IET Circuits, Devices, and Systems (2011). 2011

6. A Transient Electrothermal Analysis of Three-Dimensional Integrated Circuits

R. Harris, S. Priyadarshi, S. Melamed, **Ortega, C.** R. Manohar, N Dolley, N. Kriplani, W. Davis, P. Franzon, M Steer

IEEE Transactions of Components and Packagign Technologies (2011). 2011

7. Static Power Reduction Techniques for Asynchronous Circuits

Ortega, C. J. Tse, R. Manohar

International Symposim on Asynchronous Circuits and Systems (ASYNC) (2010). 2010

8. Variability in 3-D Integrated Circuits

F. Akopyan, **Ortega, C.** D. Fang, Jackson S.. R. Manohar

Custom Integrated Circuits Conference (CICC) (2008). 2008

8. Estimacion de Consumo de Potencia Dinamica de un μcroprocesador Superescalar

M. De Alba, I. Cabrera, **Ortega, C.**

Encuentro Nacional de Investigacion de Ingeneria Electrica (ENINVIE) (2005). 2005

awards

2006-2009	**CONACyT-Cornell Fellowship for Doctoral studies**	CONACyT
2005	**IUERI Undergraduate Research Internship**	Cornell University
2002-2004	**ITESM-CEM scholarship for Undergraduates**	ITESM-CEM
2004	**Travel grant: XXIX Pan-american Engineering Convention**	ITESM-CEM

professional service

2013	**Panelist**	TAPIA
	Panel on Cybersecurity as a representative of the TRUST center	
2008,2013-16	**Reviewer**	ASYNC
2014	**Reviewer**	Integration, The VLSI Journal

skills

- **Innovation**. Large-scale engineering, multidisciplinary outreach, education
- **Circuit Design**. Verilog, VHDL, HSPICE, HSIM, UltraSim, Calibre, Cadence, Encounter, Eagle, PCB, Xilinx ISE, LTSpice, laboratory equipment
- **Computer Technology**. Python, C, Java, Perl, TCL, Skill(some), C++(some), Unix tools, XML, and many more
- **Ubiquitous computing**. Kinetis, ARM Cortex-M0+, AVR, Arduino, MSP430, Raspberry-PI