# Static Power Reduction Techniques for Asynchronous Circuits

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AVLSI

## Low Duty Cycle IC

- Biological Implants
- Neurological stimulators
- Cardiac rythm management
- RFID tags
- Remote sensing devices

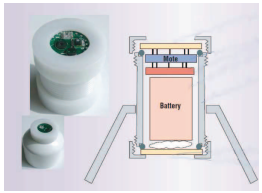



Fig.1: Berkeley Microweather station

- We need little power consumption during idle times
- Spend a lot of time idle
- No room for overheads
- Bursty Operation

## Leakage Mechanisms

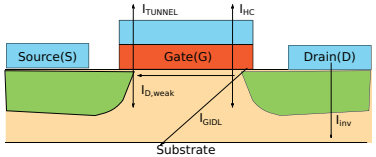



Fig.2: Leakage Mechanisms

- Source-Drain Leakage:
  - >Subthreshold Leakage ($I_{D,WEAK}$)
  - >Reverse biased diode lekage ($I_{inv}$)
  - >Gate-Induced Drain Leakage ($I_{GIDL}$)
- Gate Leakage:
  - >Direct Tunneling ($I_{TUNNEL}$)
  - >Hot Carrier Injection ($I_{HC}$)

## Impact of CMOS Scaling in Static Power

- Leakage expected to increase
- Major Concerns
  - > Tox scaling, channel miniaturization
  - > Vdd, Vth scaling

## Static Power Reduction Techniques

- Device level
  - > Doping halo and concentration
  - > Nominal values of $V_{th}$ and $V_{dd}$
- Circuit level
  - > Natual and forced stacking
- System level
  - > Power Gating

## Power Gating

- Series Resistance
  - Leakage reduction
  - Performance penalty
- Virtual Power Nets
  - Virtual VDD - *gvddv*
  - Virtual GND - *gvssv*

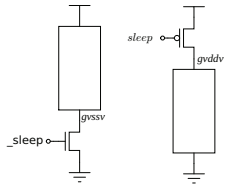



Fig.3: Power Gating

### *Non-State Preserving Power Gating*

- Disconnect from power during idle mode
- Internal nodes float
- Transient behavior
  - Long sleep settle time
  - Long wake-up time
- Cut-Off: CO, MTCMOS, BGMOS, SCMOS

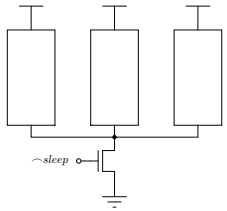



Fig.4: Non-State Preserving Power Gating

### *State Preserving Power Gating*

- Select head or foot transistor
  - Output is "0" - head transistor
  - Ouptut is "1" - foot transistor
- Better transient behavior
- Less static power reduction

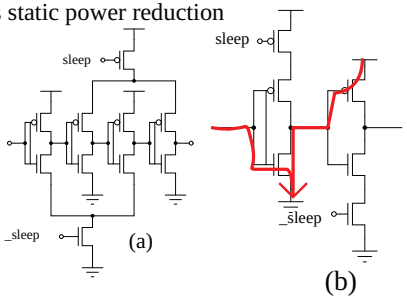



Fig.5: (a) State Preserving Power Gating,
(b) Sneak Leakage Paths

## Asynchronous Power Gating

### *Non-State Preserving Asynchronous Power Gating (CO)*

- Similar to Cut-Off technique
- Requires isolation circuitry
- Requires self reset sequence

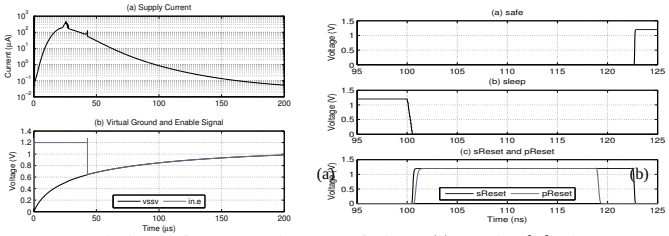



Fig.6: Non-State-Preserving Power Gating. (a) Transient behavior
(b) Self-reset sequence

### *State Preserving Asynchronous Power Gating (ZZCO, ZZCO-WS)*

- High speed asynchronous circuits heavily rely on dynamic gates
- Forward inverter uses complementary virtual power rail
- Disable staticizers during sleep mode

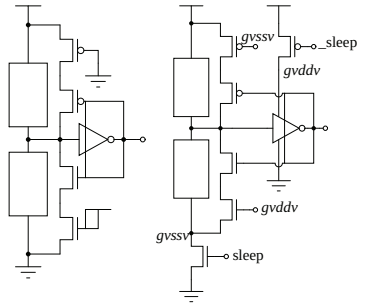



Fig.7: Disabled Staticizer

## Control Circuitry

Infrastructure to detect when it is safe to power gate a pipeline

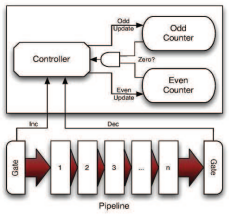



Fig.8. Empty Pipeline Detection

## Efficient Pipelined Power Gating

### Zero-Delay Ripple Turn On (ZDRTO)

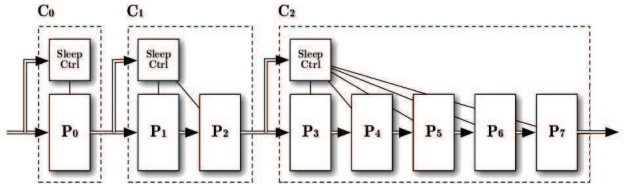



Fig.9. ZDRTO block diagram

- Hide wake-up latency of downstream stages
- Async Circuit Robustness - Do computation during power on
- Methodology
  - Partition the pipeline into clusters (power domains)
  - Distribute sleep/wakeup control

### Evaluation

***Power Gating Techniques***

- Used AES round pipeline as benchmark
  - > AK -> 8400 transistors
  - > SR -> 7600 transistors
  - > BS -> 84000 transistors
  - > MC -> 30000 transistors
- Applied technique to each component

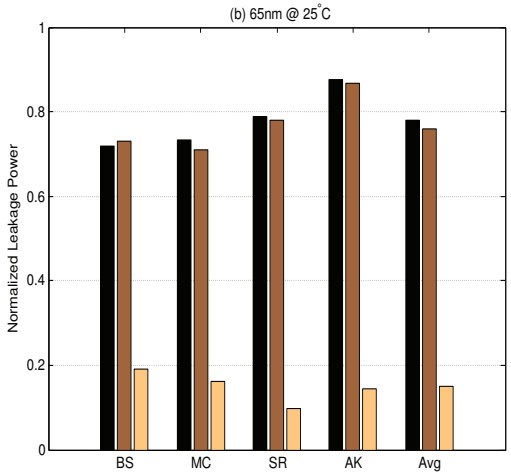



Fig.10: Normalized Leakage Power

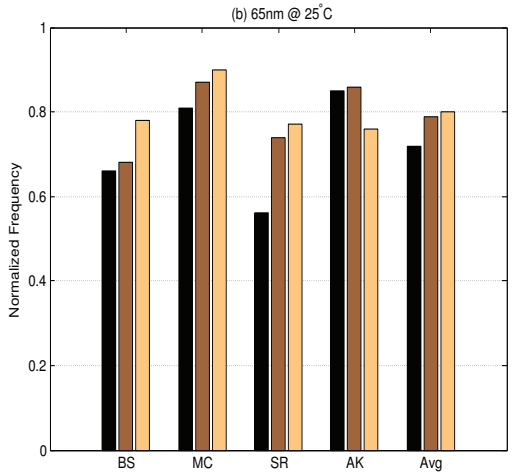



Fig.10: Normalized Frequency Penalty

***ZDRTO Evaluation***

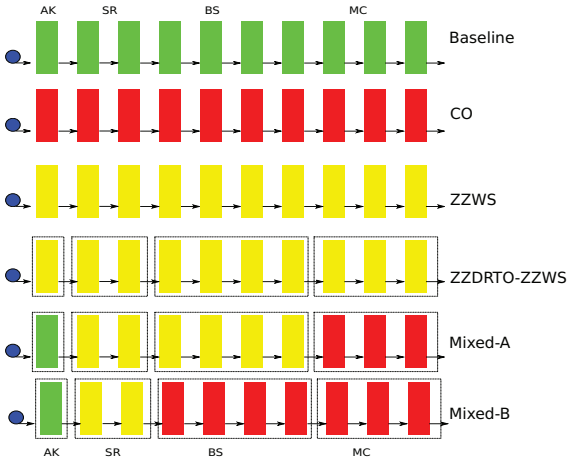
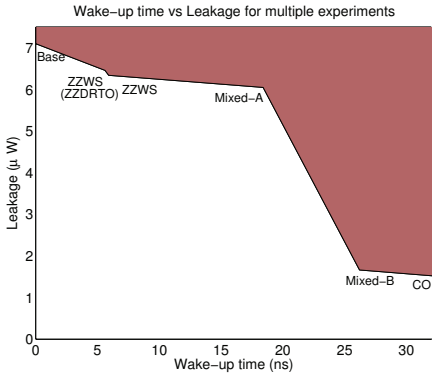



Fig 11. ZRDTO experimental setup

| | Wake up time(ns) | Static Power (uW) | Frequency (Mhz) | |
|---|---|---|---|---|
| Baseline | 0 | 7.1 | 285 | |
| CO | 32.9 | 1.5 | 262 | Non-ZRDTO |
| ZZ | 5.9 | 6.3 | 180 | |
| ZZ-ZRDTO | 5.6 | 6.4 | 182 | ZRDTO |
| Mixed-A | 18.4 | 6.0 | 226 | |
| Mixed-B | 26.1 | 1.6 | 260 | |

Table 1: ZRDTO Results




### Contributions

- Power gating techniques in asynchronous Circuits
- ZDRTO - Efficient pipelined power Gating

### Conclusions

- Analyzed leakage mechanisms
- Presented asynchronous power gating techniques
  - Static Power reductions ranging from **25%** to **80%**
- Empty pipeline detection control circuit
- ***Zero-Delay Ripple Turn On (ZDRTO)***
  - Hides wake-up latency in pipelined circuits
- Demonstrated tradeoffs between of hybrid power gating schemes

### References

•Carlos Ortega, Jonathan Tse and Rajit Manohar,
*Static Power reduction techniques for Asynchronous Circuits*
IEEE Symp. on Asynchronous Circuits and Systems(ASYNC) 2010

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### Notes